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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/780,427

02/17/2004

Chih-Ching Shih

A1351

2005

45851

7590

01/26/2006

G. VICTOR TREYZ

FLOOD BUILDING

870 MARKET STREET, SUITE 984

SAN FRANCISCO, CA 94102

EXAMINER

SOWARD, IDA M

ART UNIT

PAPER NUMBER

2822

DATE MAILED: 01/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/780,427

Applicant(s)

SHIH ET AL.

Examiner

Ida M. Soward

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 November 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3, 5-10 and 14-16 is/are rejected.
- 7) ☒ Claim(s) 4, 11-13 and 17-19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Applicants' amendment filed November 10, 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5-10 and 14-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Huang et al. (6,897,543 B1)

The applied reference has a common inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In regard to claim 1, Huang et al. teach an integrated circuit antifuse circuitry,

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comprising: a metal-insulator-semiconductor antifuse transistor having a drain 94 , source 96, gate 108, and substrate 88, wherein the drain 94 and substrate 96 form a drain-substrate p-n junction, wherein the substrate 88 and source 96 form a substrate-source p-n junction, and wherein the gate 108 has a gate insulator 106 (Figure 5, columns 7-8, lines 52-67 and 1-62, respectively).

In regard to claim 2, Huang et al. teach the gate insulator 106 comprising gate oxide (Figure 5).

In regard to claim 3, Huang et al. teach sensing circuitry (Figure 3, columns 5-6, lines 23-67 and 1-38, respectively).

In regard to claim 5, Huang et al. teach a resistor R2 connected between the substrate SUB and the source S (Figure 4).

In regard to claim 6, Huang et al. teach a conductor 92 that electrically interconnects the gate 108 and the source 96 (Figure 5, column 8, lines 4-10).

In regard to claim 7, Huang et al. teach a resistor R1 that connects the drain D to a positive supply voltage Vcc (Figure 4).

In regard to claims 8 and 16, Huang et al. teach the gate G electrically connected to the source S, the integrated circuit antifuse circuitry further comprising: a first resistor R1 connected between the drain D and a positive power supply voltage Vcc; a second resistor R2 connected between the substrate SUB and a ground potential Vss (Figure 4).

In regard to claim 9, Huang et al. teach the drain 94, source 96, and substrate 88a surrounded by an isolating well 140 (Figure 13, columns 11-12, lines 26-67 and 1-6, respectively).

In regard to claim 10, Huang et al. teach the circuitry that applies the voltages comprises at least one Zener diode connected between the drain and substrate and at least one resistor connected between the substrate and the source, wherein the Zener diode is reverse biased and breaks down to allow current to flow from the Zener diode through the resistor to help forward bias the substrate-source p-n junction (Figure 8, column 9, lines 58-67).

In regard to claim 1 and 3, Huang et al. teach the functional language of the claims directed to structure (columns 2-3 and 6, lines 63-67, 1-9 and 10-27, respectively).

In regard to claim 14, "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985). See MPEP § 2113.

In regard to claim 15, Huang et al. teach the circuitry that applies the voltages is formed on an integrated circuit having I/O circuitry powered by an I/O power supply

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voltage, wherein the circuitry that applies the voltages applies the 1/0 power supply voltage to the drain (column 14, lines 16-21).

Allowable Subject Matter

Claims 4, 11-13 and 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to integrated circuit antifuse circuitry structures:

Kothandaraman (US 2003/0169095 A1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ida M. Soward whose telephone number is 571-272-

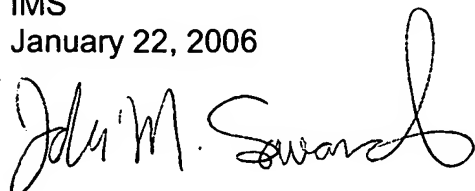
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1845. The examiner can normally be reached on Monday - Thursday 6:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra V. Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

IMS
January 22, 2006


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